IN THE CLAIMS

1 (Currently Amended). A method of forming a semiconductor structure comprising:

providing a single crystal semiconductor substrate of GaP; and

fabricating a graded composition buffer including a plurality of epitaxial semiconductor $In_x(Al_yGa_{1-y})_{1-x}P$ alloy layers where y is greater than zero, said buffer comprising a first alloy layer immediately contacting the substrate having a lattice constant that is nearly identical to that of the substrate and a growth temperature greater than 650°C, subsequent alloy layers having lattice constants that differ from adjacent layers by less than 1%, and a final alloy layer having a lattice constant that is substantially different from the substrate, wherein growth temperature of the final alloy layer is at least 20°C less than the growth temperature of the first alloy layer.

2 (Original). The method of claim 1, wherein growth temperature is decreased in at least one discrete transition during the growth of the graded composition buffer.

3 (Original). The method of claim 1, wherein the growth temperature of the first alloy is greater than or equal to 710°C.

4 (Original). The method of claim 2, wherein the growth temperature of the first alloy is greater than or equal to 710°C.

5 (Original). The method of claim 4, wherein first discrete transition in growth temperature ends in a growth temperature of 700° C or lower and occurs at a composition where x is between 0.05 and 0.35.

6 (Original). The method of claim 5, wherein a second discrete transition in growth temperature ends in a growth temperature of 650°C or lower and occurs at a composition where x is between 0.2 and 0.35.

7 (Original). The method of claim 6, wherein a third discrete transition in growth temperature ends in a growth temperature of 650°C or lower and occurs at a composition where x is between 0.3 and 0.6.

8 (Original). The method of claim 4, wherein a plurality of subsequent discrete transitions in growth temperature ends in a final growth temperature between 575 and 700°C.

9 (Original). The method of claim 4, wherein a plurality of subsequent discrete transitions in growth temperature ends in a final growth temperature between 480 and 560°C.

10 (Original). The method of claim 4, wherein a first discrete transition in growth temperature ends in a growth temperature of 560°C or lower and occurs at a composition where x is between 0.1 and 0.35.

11 (Original). The method of claim 2, wherein the growth temperature of the first alloy layer is greater than or equal to 750°C, a first discrete transition in growth temperature ends in a growth temperature of 675°C and occurs at a composition where $x=0.18$.

12 (Original). The method of claim 11 wherein a second discrete transition in growth temperature ends in a growth temperature of 650°C and occurs at a composition where $x=0.27$.

13 (Original). The method of claim 12, wherein a third discrete transition in growth temperature ends in a growth temperature of 625°C and occurs at a composition where $x=0.4$.

14 (Original). The method of claim 11, wherein a second discrete transition in growth temperature ends in a growth temperature between 525 and 550°C and occurs at a composition where x is between 0.25 and 0.35.

15 (Original). The method of claim 2, wherein the growth temperature of the first alloy layer is greater than or equal to 760°C, a first discrete transition in growth temperature ends in a growth temperature between 525 and 550°C and occurs at a composition where $x=0.18$.

16 (Original). The method of claim 1, wherein the substrate and the graded composition buffer are electrically doped with elements.

17 (Original). The method of claim 16, wherein the dopant elements comprise n-type dopants.

18 (Original). The method of claim 17, wherein the dopant element in the graded composition buffer comprises Si.

19 (Original). The method of claim 16, wherein the dopant elements comprise p-type dopants.

20 (Original). The method of claim 16, wherein the concentration of the dopant element in the alloy layers of the graded composition buffer is between $5x10^{16}$ and $5x10^{18}$ cm^{-3}.

21 (Original). The method of claim 18 wherein the concentration of Si in the alloy layers of the graded composition buffer is between $1x10^{17}$ and $5x10^{18}$ cm^{-3}.

22 (Original). The method of claim 2 wherein the substrate is electrically doped with an n-type dopant, the graded composition buffer is electrically doped with Si at a concentration between $1x10^{17}$ and $2x10^{18}$ cm^{-3}, the growth temperature of the first alloy layer is greater than

or equal to 750°C, a first discrete transition in growth temperature ends in a growth temperature of 700°C or lower and occurs at a composition where x is between 0.13 and 0.2.

23 (Original). The method of claim 1, wherein aluminum is present in the alloys ($y > 0$) such that the grade composition buffer is transparent to light emitted or absorbed by $In_xGa_{1-x}P$ lattice-matched to the final alloy layer.

24 (Original). The method of claim 23, wherein aluminum concentration in the alloy layers is such that y equals or is greater than 0.02.

25 (Original). The method of claim 23, wherein y equals or is greater than 0.05 beginning at a composition where x equals or is greater than 0.25.

26 (Original). The method of claim 23, wherein y equals or is greater than 0.05 beginning at a composition where x is at least 0.02 less than it is in the final alloy layer.

27 (Original). The method of claim 1, wherein semiconductor layers are incorporated on the graded composition buffer, and said layers comprise at least one strain-balancing semiconductor layer with nominally the same coefficient of thermal expansion as GaP.

28 (Original). The method of claim 27, wherein the strain balancing semiconductor layer comprises $In_x(Al_yGa_{1-y})_{1-x}P$ with a lattice constant smaller than that of the final alloy layer of the grade composition buffer.

29 (Original). The method of claim 28, wherein the strain balancing semiconductor layer is at least 5 microns in thickness.

30 (Original). The method of claim 27, wherein the strain balancing semiconductor layer comprises GaP.

31 (Previously Amended). The method claim of claim 27, wherein the strain balancing semiconductor layer comprises an epitaxial layer.

32 (Previously Amended). The method claim of claim 27, wherein the strain balancing semiconductor layer comprises a wafer-bonded layer.

33 (Original). The method of claim 30, wherein the strain-balancing semiconductor layer is at least 5 microns in thickness.

34 (Original). The method of claim 1, wherein additional layers are deposited on the graded composition buffer in order to fabricate optoelectronic devices thereon.

35 (Original). The method of claim 34, wherein at least one of the additional layers is an active layer whose purpose is to emit or absorb light.

36 (Original). The method of claim 35, wherein aluminum is present ($y > 0$) in the alloy layers of the graded composition buffer such that the graded composition buffer is transparent to light emitted or absorbed by the active layer or active layers.

37 (Original). The method of claim 36, wherein aluminum concentration in the alloy layers of the graded composition buffer is such that y equals or is greater than 0.02.

38 (Original). The method of claim 37, wherein y equals or is greater than 0.05 beginning at a composition where x equals or is greater than 0.25.

39 (Original). The method of claim 38, wherein y equals or is greater than 0.05 beginning at a composition where x is at least 0.02 less than it is in the final alloy layer of the graded composition buffer.

40 (Original). The method of claim 34, wherein the optoelectronic devices comprise light-emitting diodes.

41 (Original). The method of claim 34, wherein the optoelectronic devices comprise laser diodes.

42 (Original). The method of claim 34, wherein the optoelectronic devices comprise photodetectors.

43 (Original). The method of claim 34, wherein the optoelectronic devices comprise photocathodes.

44 (Original). The method of claim 34, wherein the optoelectronic devices comprise modulators.

45 (Original). The method of claim 1, wherein the alloy layers in the graded composition buffer comprise indium gallium phosphide where the lattice constant differs between adjacent layers by less than 0.2%, the substrate is electrically doped with an n-type dopant, the graded composition buffer is electrically doped with Si to a concentration of $7x10^{17}$ cm^{-3}, the first alloy layer of the graded composition buffer is grown at 800°C, the first discrete transition in growth temperature ends in a growth temperature of 675°C and occurs at a composition where $x=0.18$, the second discrete transition in growth temperature ends in a growth temperature of 650°C and occurs at a composition where $x=0.26$.

46 (Original). The method of claim 45, wherein a light-emitting diode is deposited after the final alloy layer of the graded composition buffer.

47 (Original). The method of claim 45, wherein a light-emitting diode is deposited after the final alloy layer of the graded composition buffer and a GaP strain-balancing layer is deposited with a thickness of at least 5 microns.

48 (Original). The method of claim 45, wherein a third discrete transition in growth temperature ends in a growth temperature of 625°C and occurs at a composition where $x=0.40$.

49 (Original). The method of claim 48, wherein a light-emitting diode is deposited after the final alloy layer of the graded composition buffer.

50 (Original). The method of claim 48, wherein a light-emitting diode is deposited after the final alloy layer of the graded composition buffer and a GaP strain-balancing layer is deposited with a thickness of at least 5 microns.

51 (Original). The method of claim 1, wherein the alloy layers in the graded composition buffer comprise indium gallium phosphide where the lattice constant differs between adjacent layers by less than 0.2%, the substrate is electrically doped with an n-type

dopant, the graded composition buffer is electrically doped with Si to a concentration of $7x10^{17}$ cm^{-3}, the first alloy layer of the graded composition buffer is grown at 800°C, the first discrete transition in growth temperature ends in a growth temperature of 675°C and occurs at a composition where $x=0.18$, and aluminum composition in the alloy layers is $y=0.15$ for alloy compositions greater than or equal to $x=0.25$.

52 (Original). The method of claim 51, wherein additional layers are deposited on the final alloy layer of the graded composition buffer.

53 (Original). The method of claim 52, wherein the additional layers form the structure for a light-emitting diode.

54 (Original). The method of 53, wherein a strain-balancing GaP layer at least 5 microns in thickness is deposited on the light-emitting diode structure.

55 (Currently Amended). A semiconductor structure comprising:

a single crystal semiconductor substrate of GaP; and

a graded composition buffer including a plurality of epitaxial semiconductor $In_x(Al_yGa_{1-y})_{1-x}P$ alloy layers where y is greater than zero, said buffer comprising a first alloy layer immediately contacting the substrate having a lattice constant that is nearly identical to that of the substrate and a growth temperature greater than 650°C, subsequent alloy layers having

lattice constants that differ from adjacent layers by less than 1%, and a final alloy layer having a lattice constant that is substantially different from the substrate, wherein growth temperature of the final alloy layer is at least 20°C less than the growth temperature of the first alloy layer.

56 (Currently Amended). A method of forming a semiconductor structure comprising:

providing a single crystal semiconductor substrate of GaP; and

fabricating a graded composition buffer including a plurality of epitaxial semiconductor $In_x(Al_yGa_{1-y})_{1-x}P$ alloy layers where y is greater than zero, said buffer comprising a first alloy layer immediately contacting the substrate having a lattice constant that is nearly identical to that of the substrate, subsequent alloy layers having lattice constants that differ from adjacent layers by less than 1%, and a final alloy layer having a lattice constant that is substantially different from the substrate, wherein growth temperature of the final alloy layer is at least 20°C less than the growth temperature of the first alloy layer.